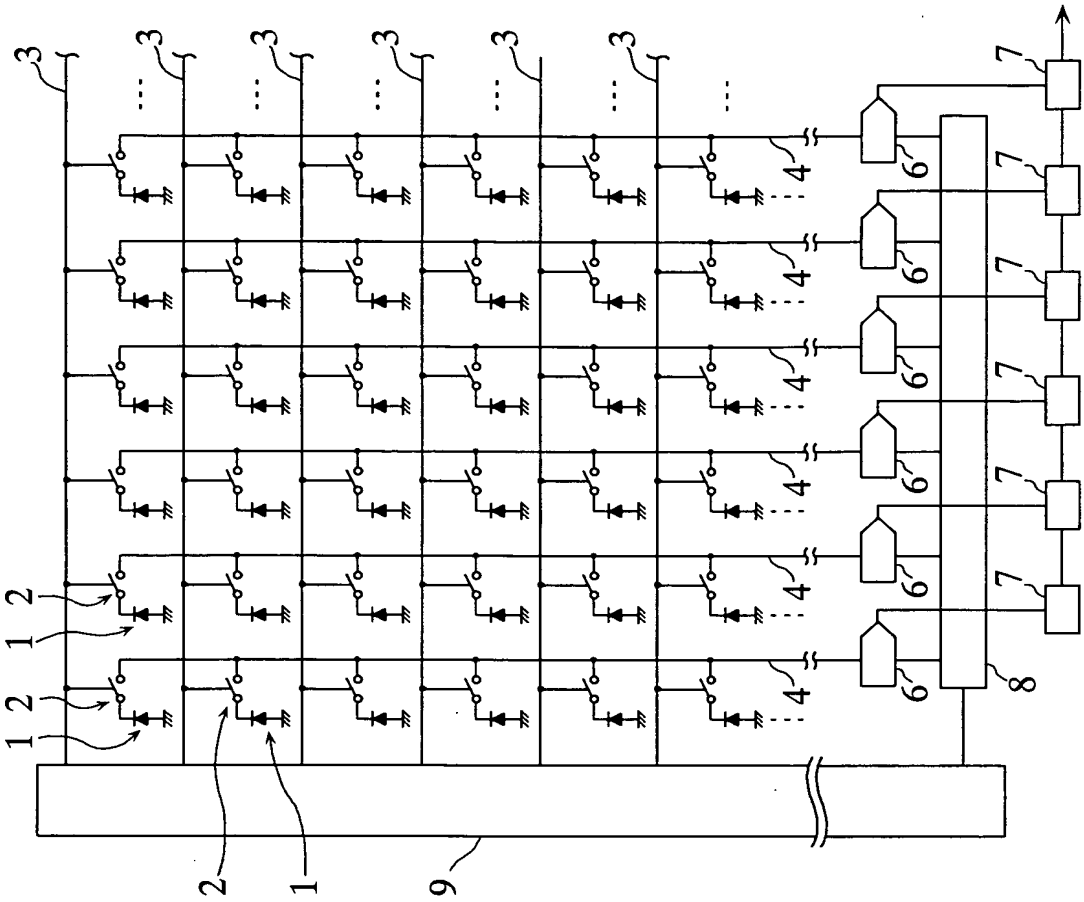
FIG.1



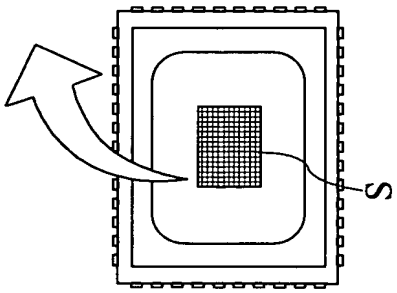



FIG.2

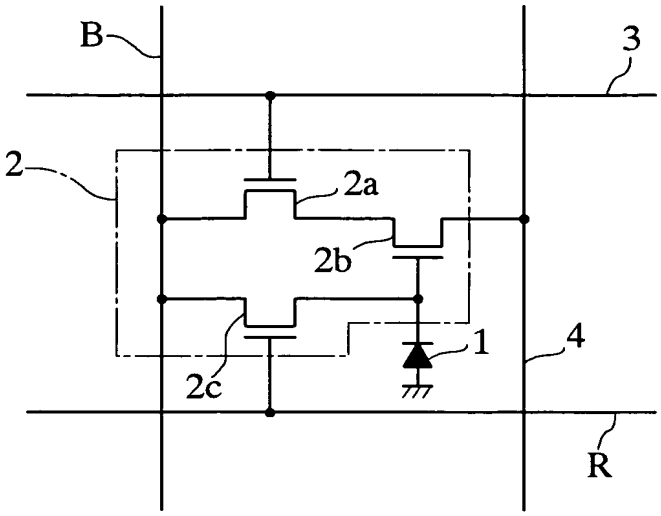

B
3
2
2a
2b
2c
1
4
R

FIG.3

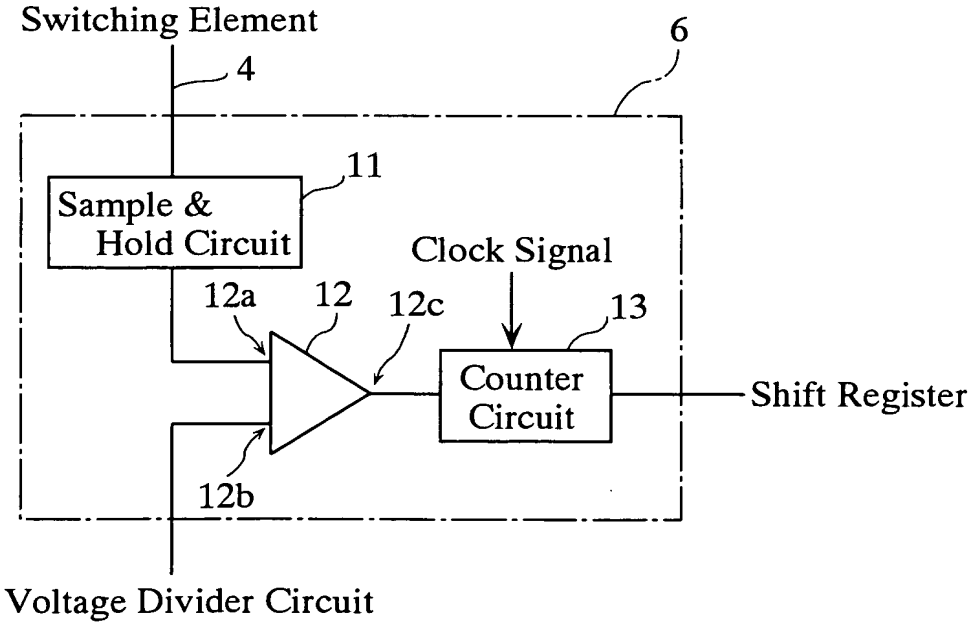

Switching Element
4
6
11
Sample &
Hold Circuit
Clock Signal
12a
12
12c
13
Counter
Circuit
Shift Register
12b
Voltage Divider Circuit

FIG.4

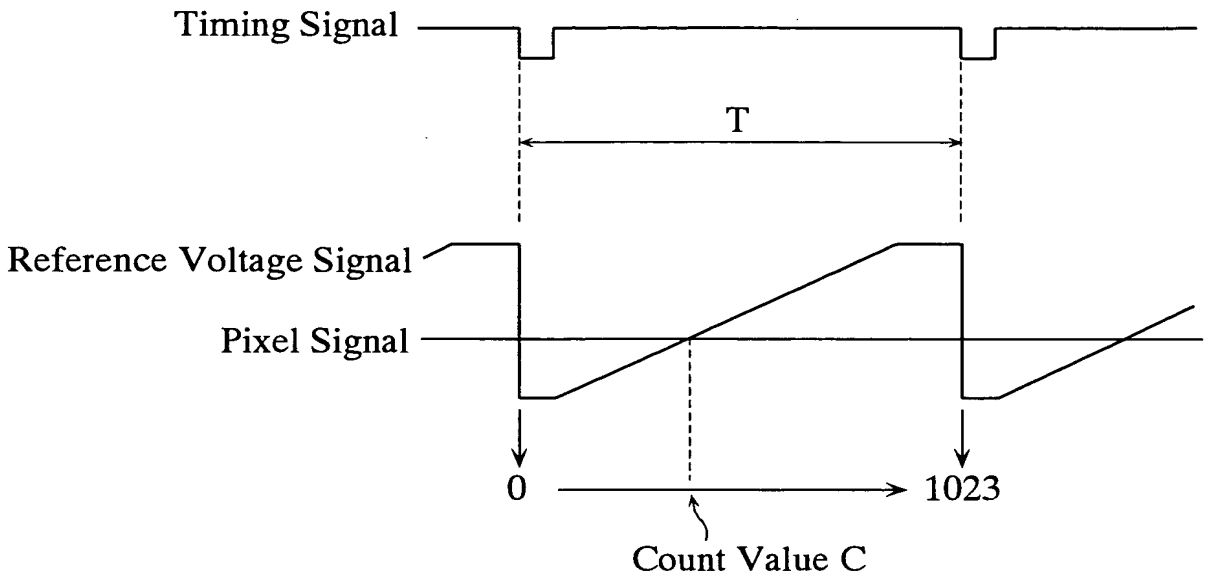

Timing Signal
T
Reference Voltage Signal
Pixel Signal
0
1023
Count Value C

FIG.5

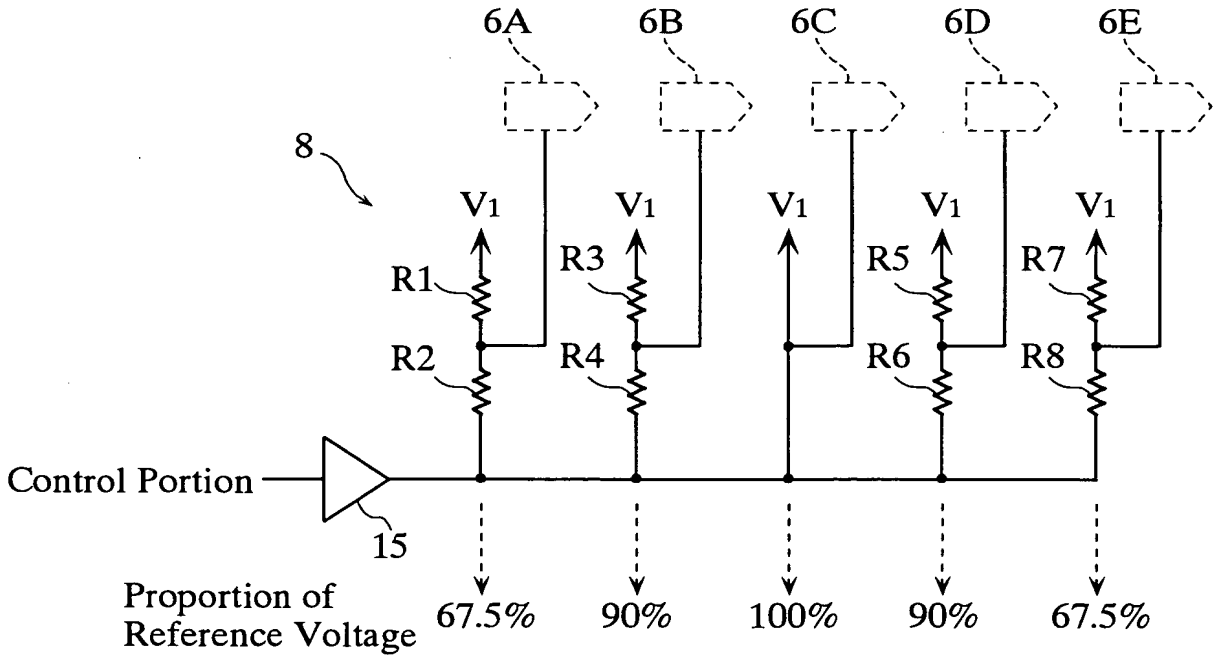

6A
6B
6C
6D
6E
8
V1
V1
V1
V1
V1
R1
R3
R5
R7
R2
R4
R6
R8
Control Portion
15
Proportion of
Reference Voltage
67.5%
90%
100%
90%
67.5%

FIG.6

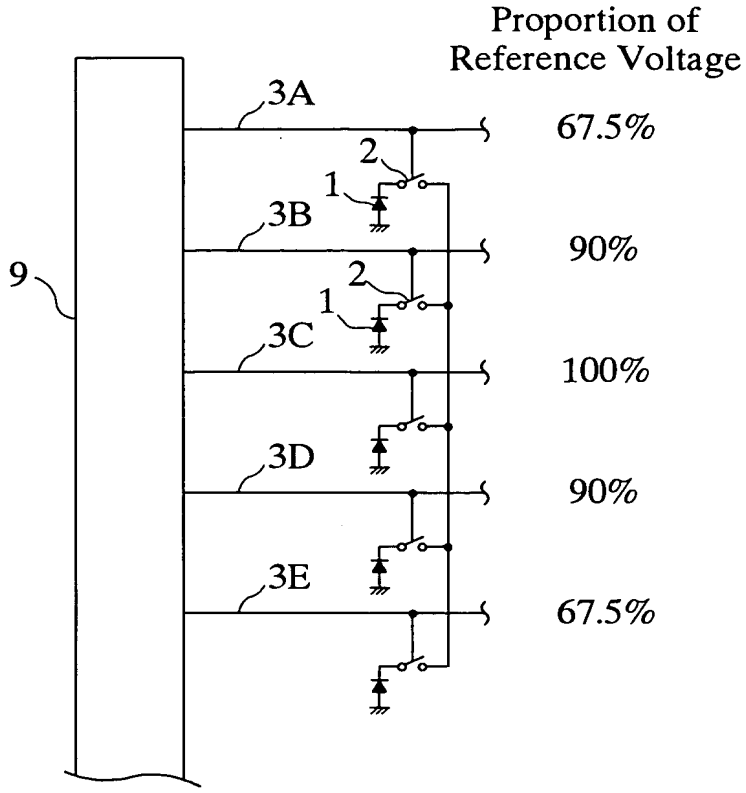

Proportion of
Reference Voltage
3A
67.5%
2
1
3B
90%
9
2
1
3C
100%
3D
90%
3E
67.5%

FIG.7

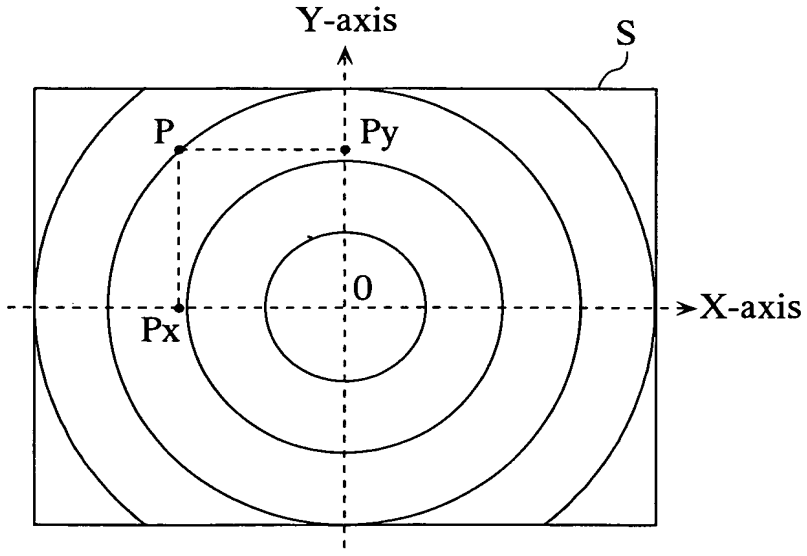

Y-axis
S
P
Py
0
Px
X-axis

FIG.8

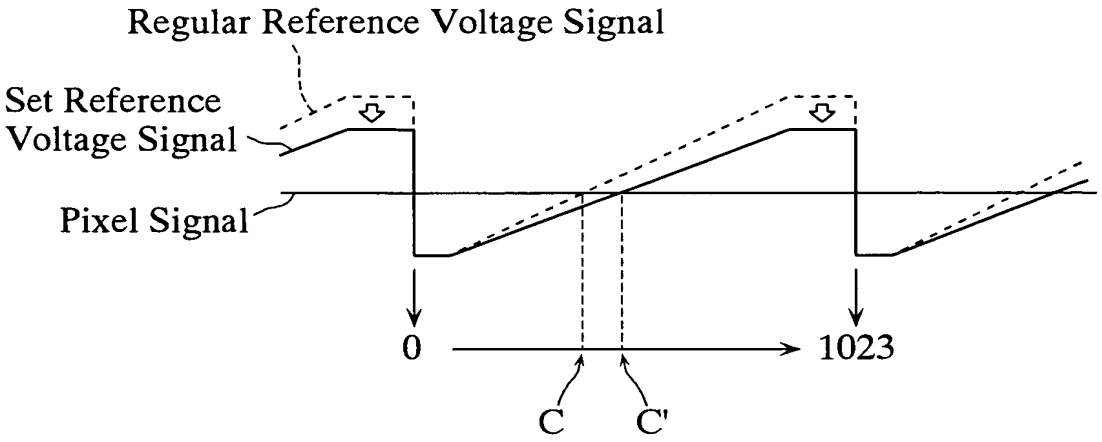

Regular Reference Voltage Signal
Set Reference
Voltage Signal
Pixel Signal
0
1023
C
C'

FIG.9

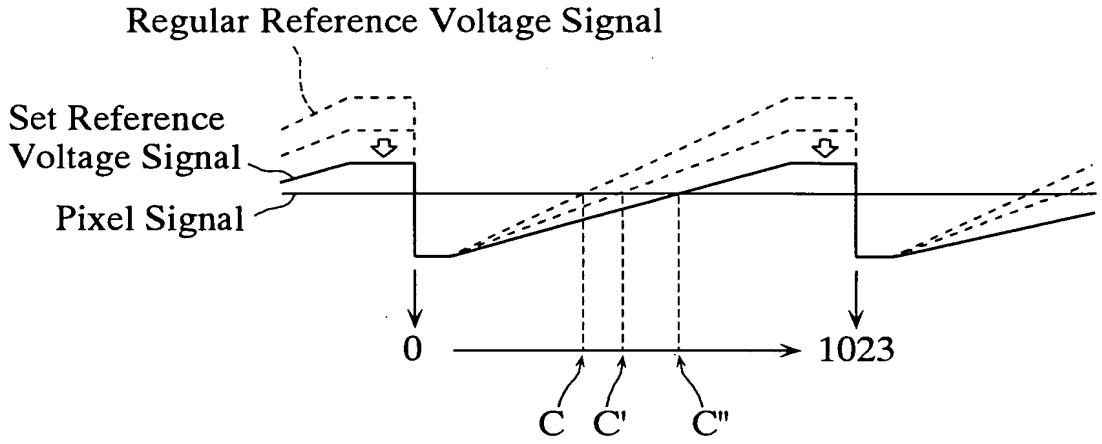

Regular Reference Voltage Signal
Set Reference
Voltage Signal
Pixel Signal
0
1023
C
C'
C''

FIG.10

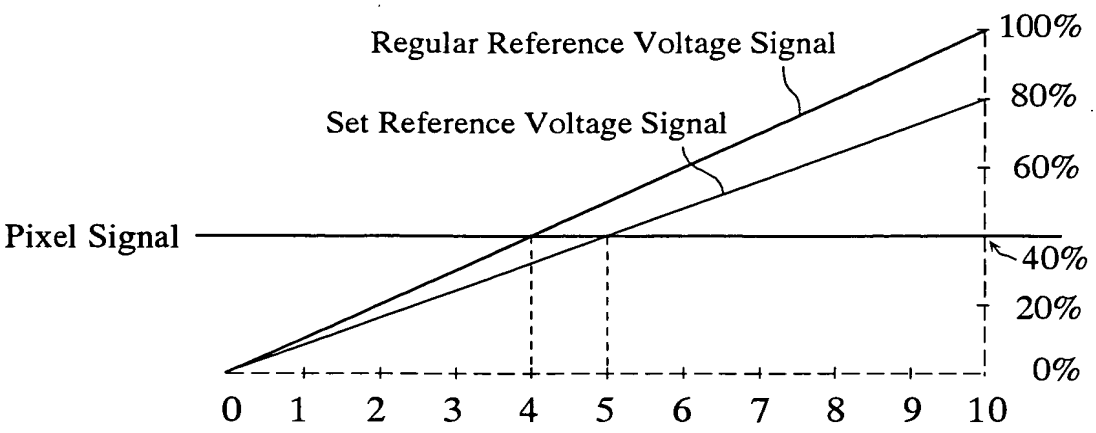

Regular Reference Voltage Signal
Set Reference Voltage Signal
Pixel Signal
100%
80%
60%
40%
20%
0%
0 1 2 3 4 5 6 7 8 9 10

FIG.11

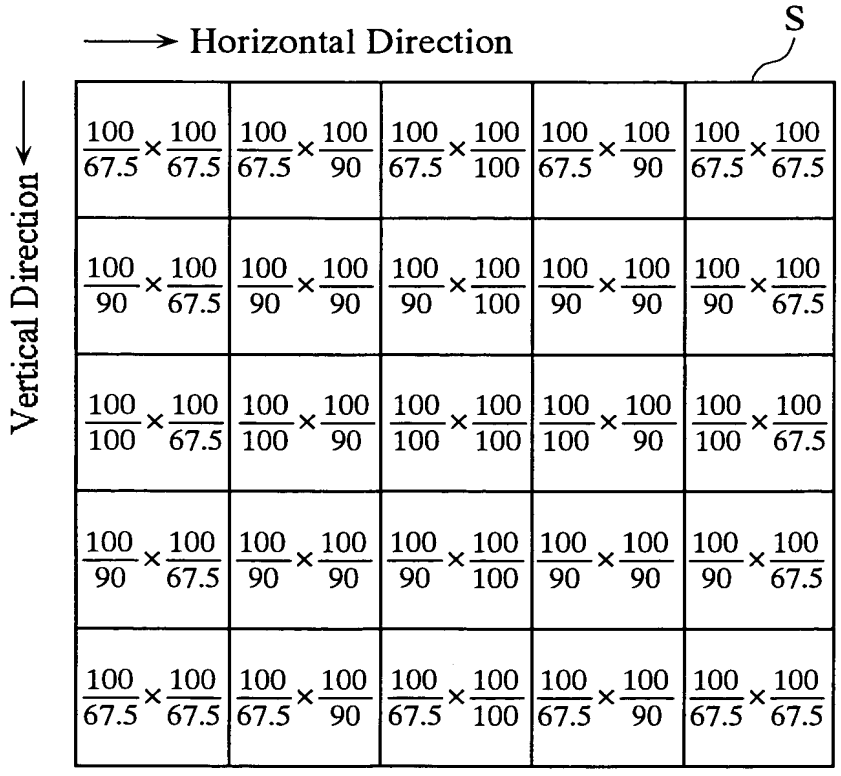

Horizontal Direction
S
Vertical Direction
100/67.5 × 100/67.5 | 100/67.5 × 100/90 | 100/67.5 × 100/100 | 100/67.5 × 100/90 | 100/67.5 × 100/67.5
100/90 × 100/67.5 | 100/90 × 100/90 | 100/90 × 100/100 | 100/90 × 100/90 | 100/90 × 100/67.5
100/100 × 100/67.5 | 100/100 × 100/90 | 100/100 × 100/100 | 100/100 × 100/90 | 100/100 × 100/67.5
100/90 × 100/67.5 | 100/90 × 100/90 | 100/90 × 100/100 | 100/90 × 100/90 | 100/90 × 100/67.5
100/67.5 × 100/67.5 | 100/67.5 × 100/90 | 100/67.5 × 100/100 | 100/67.5 × 100/90 | 100/67.5 × 100/67.5

FIG.12

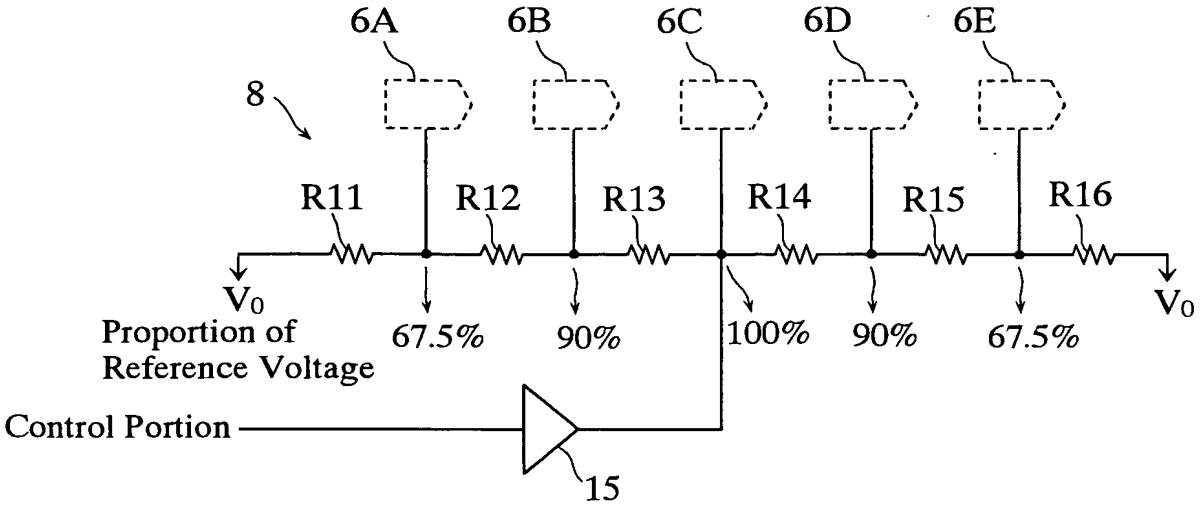

6A
6B
6C
6D
6E
8
R11
R12
R13
R14
R15
R16
V0
V0
Proportion of
Reference Voltage
67.5%
90%
100%
90%
67.5%
Control Portion
15

FIG.13

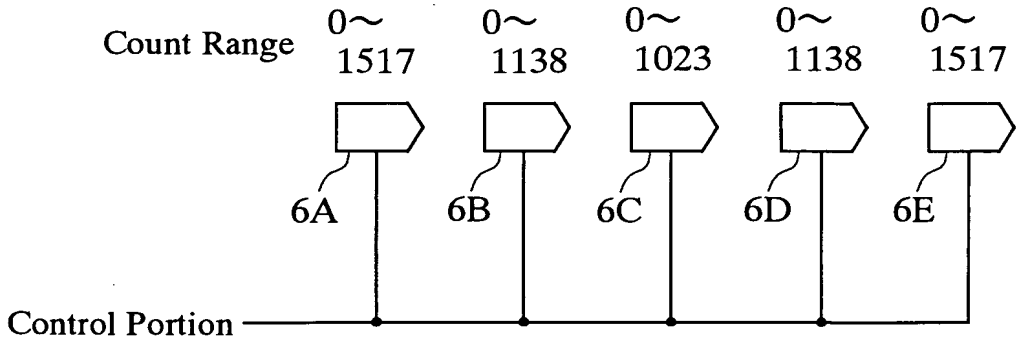

Count Range
0~
1517
0~
1138
0~
1023
0~
1138
0~
1517
6A
6B
6C
6D
6E
Control Portion

FIG.14

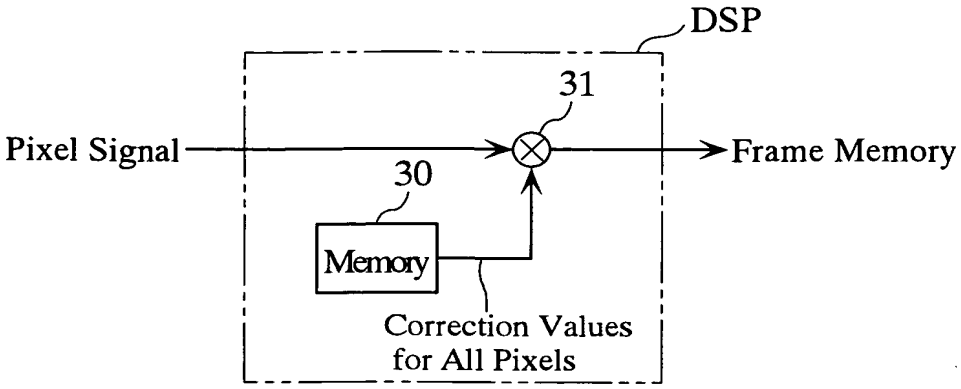



FIG.15

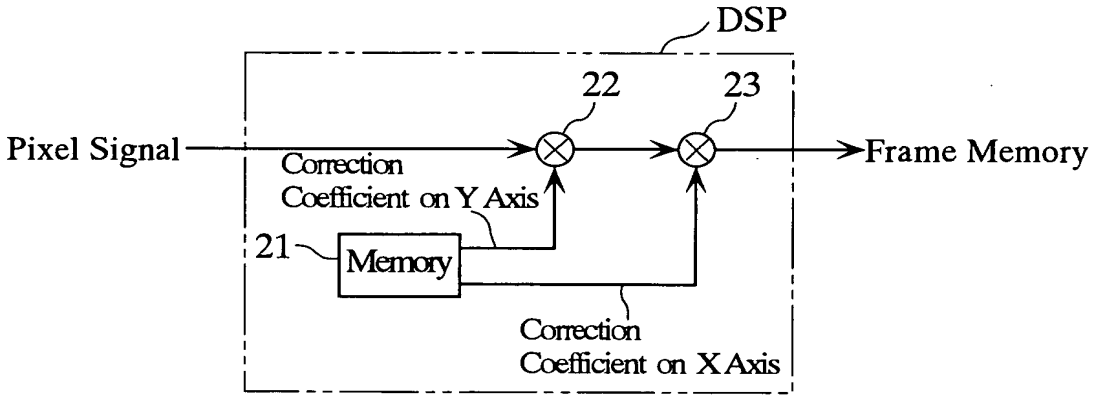



FIG.16

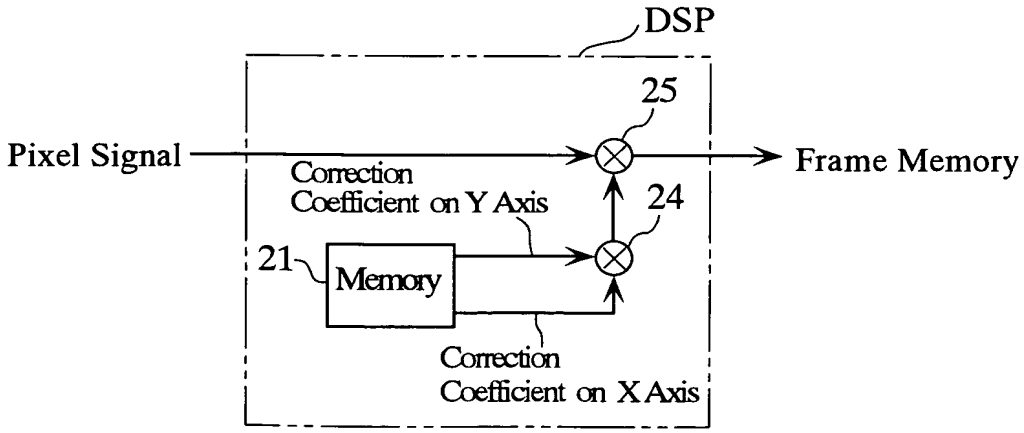


FIG.17

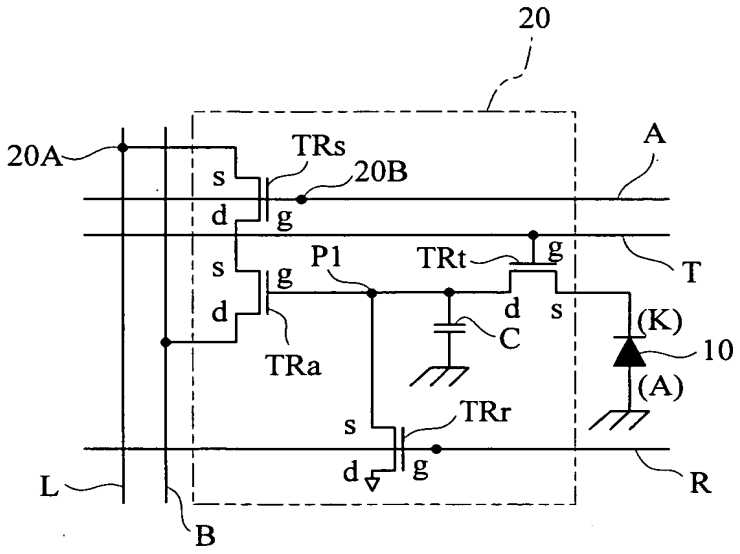


FIG.18

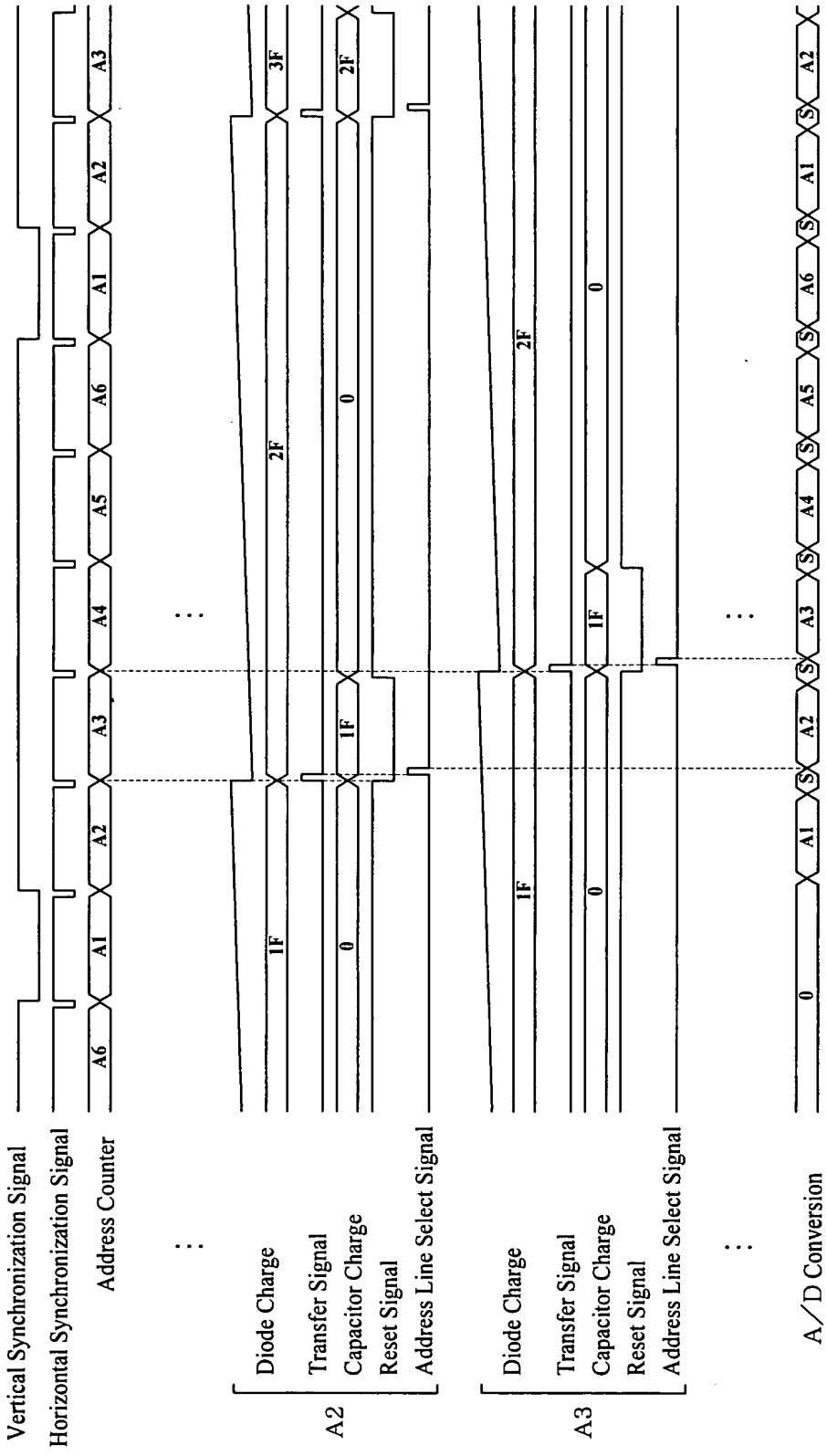

Vertical Synchronization Signal
Horizontal Synchronization Signal
Address Counter
A6
A1
A2
A3
A4
A5
A6
A1
A2
A3
A2
Diode Charge
Transfer Signal
Capacitor Charge
Reset Signal
Address Line Select Signal
1F
2F
3F
0
1F
0
2F
A3
Diode Charge
Transfer Signal
Capacitor Charge
Reset Signal
Address Line Select Signal
1F
2F
0
1F
0
A/D Conversion
0
A1
A2
A3
A4
A5
A6
A1
A2

FIG.19

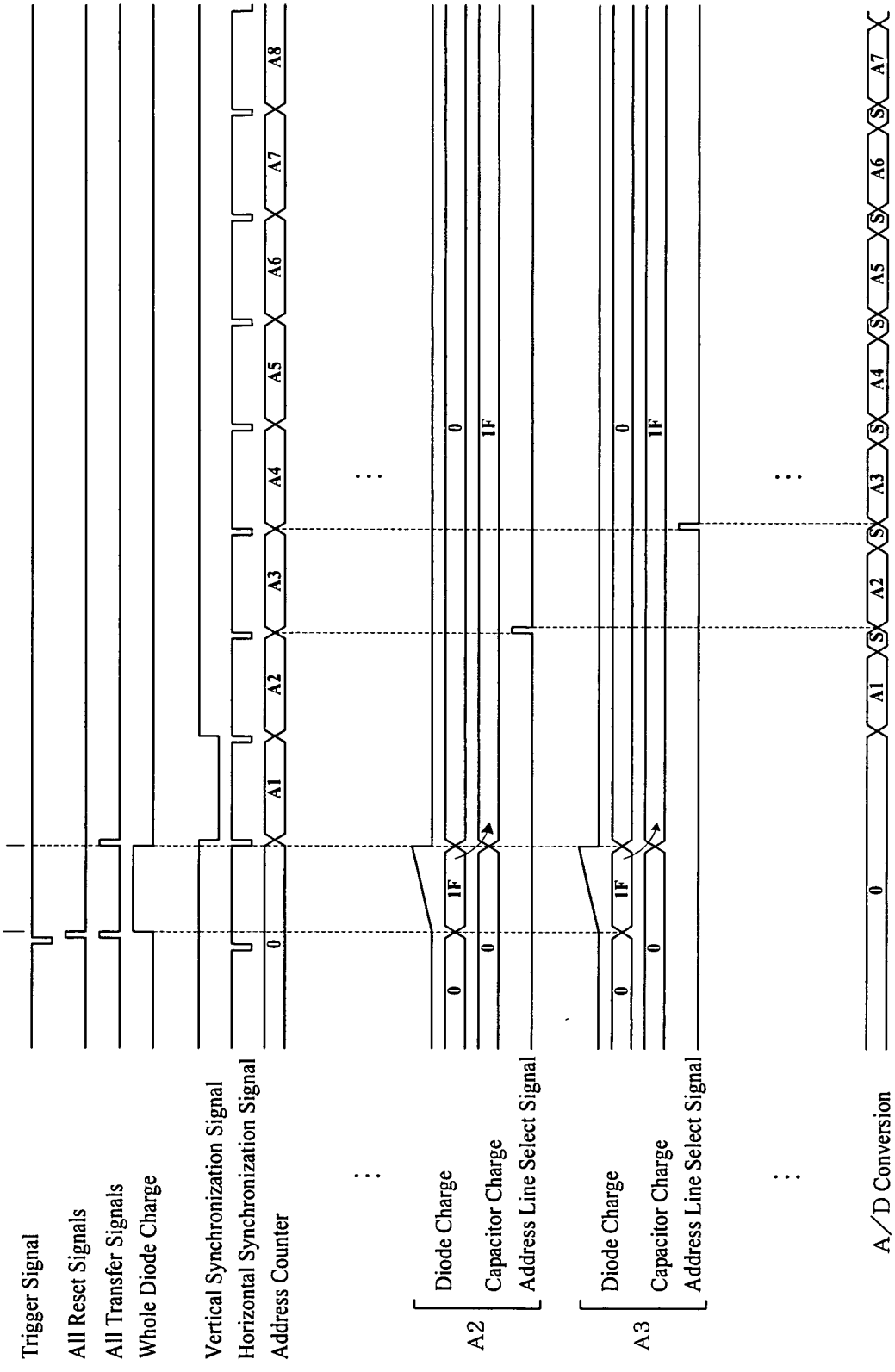

a
b
Trigger Signal
All Reset Signals
All Transfer Signals
Whole Diode Charge
Vertical Synchronization Signal
Horizontal Synchronization Signal
Address Counter
0
A1
A2
A3
A4
A5
A6
A7
A8
A2
Diode Charge
Capacitor Charge
Address Line Select Signal
0
1F
A3
Diode Charge
Capacitor Charge
Address Line Select Signal
A/D Conversion
S

FIG.20

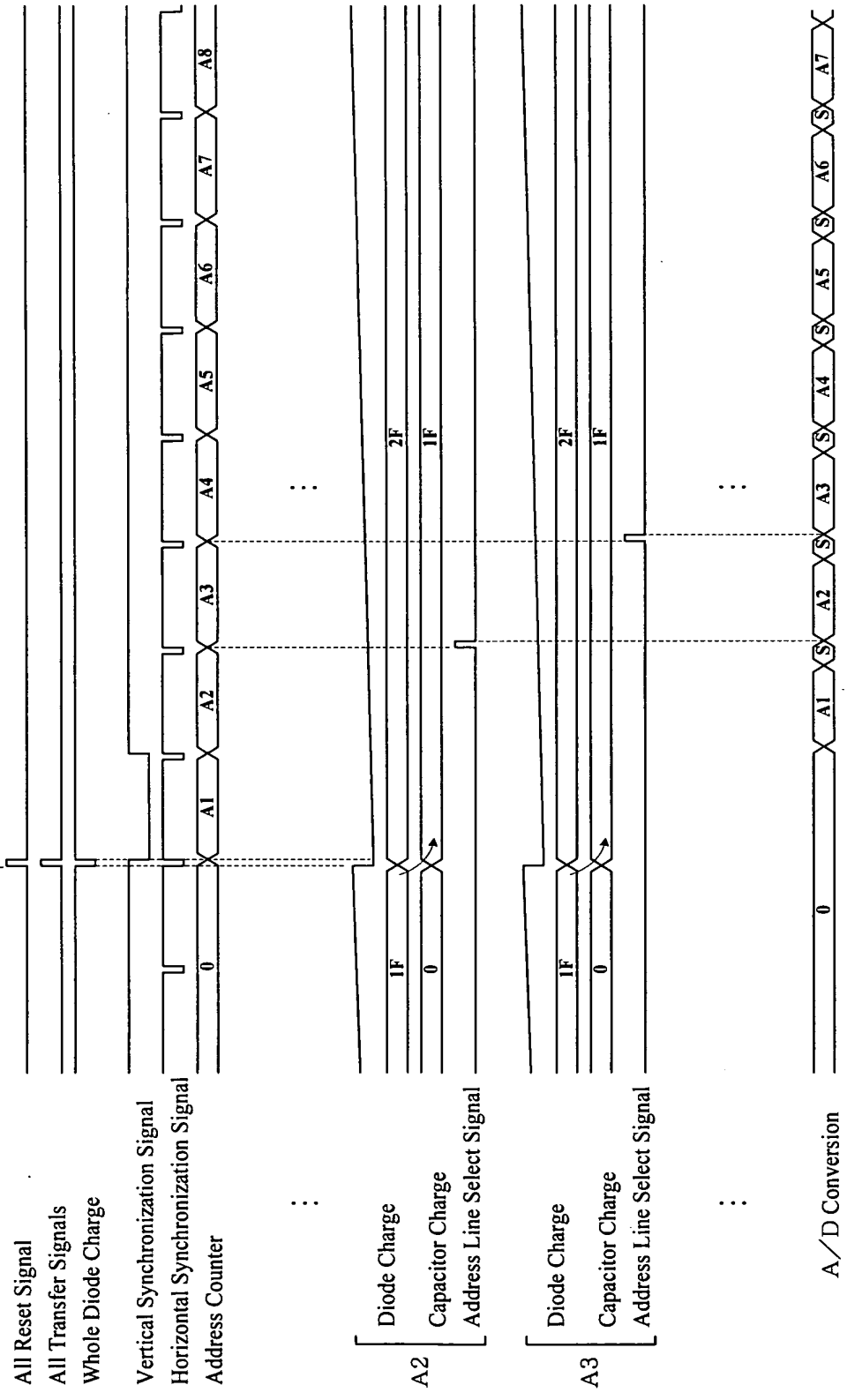

a
All Reset Signal
All Transfer Signals
Whole Diode Charge
Vertical Synchronization Signal
Horizontal Synchronization Signal
Address Counter
0
A1
A2
A3
A4
A5
A6
A7
A8
A2
Diode Charge
Capacitor Charge
Address Line Select Signal
1F
2F
0
A3
Diode Charge
Capacitor Charge
Address Line Select Signal
1F
2F
0
A/D Conversion
0
A1
A2
A3
A4
A5
A6
A7
S

FIG.21

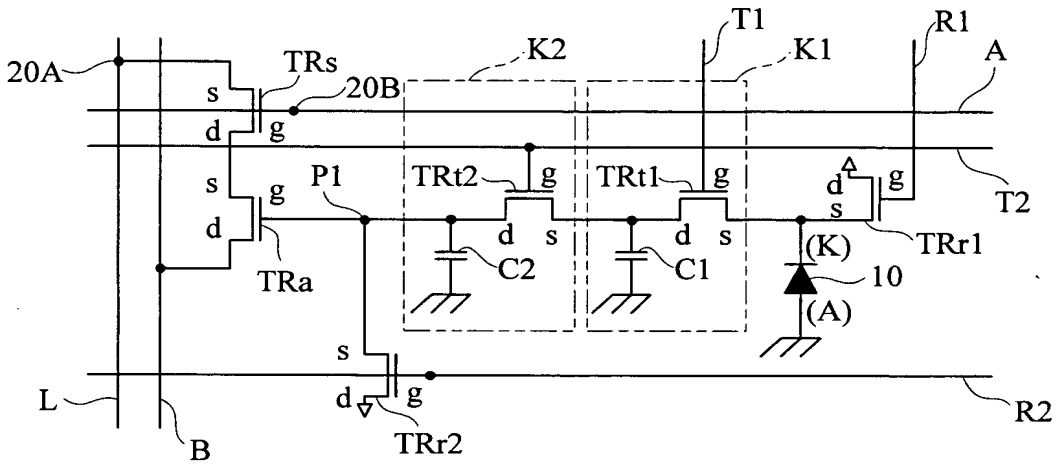

20A
TRs
20B
K2
T1
K1
R1
A
s
d
g
P1
TRt2
TRt1
T2
TRa
C2
C1
(K)
10
TRr1
(A)
L
B
TRr2
R2

FIG.22

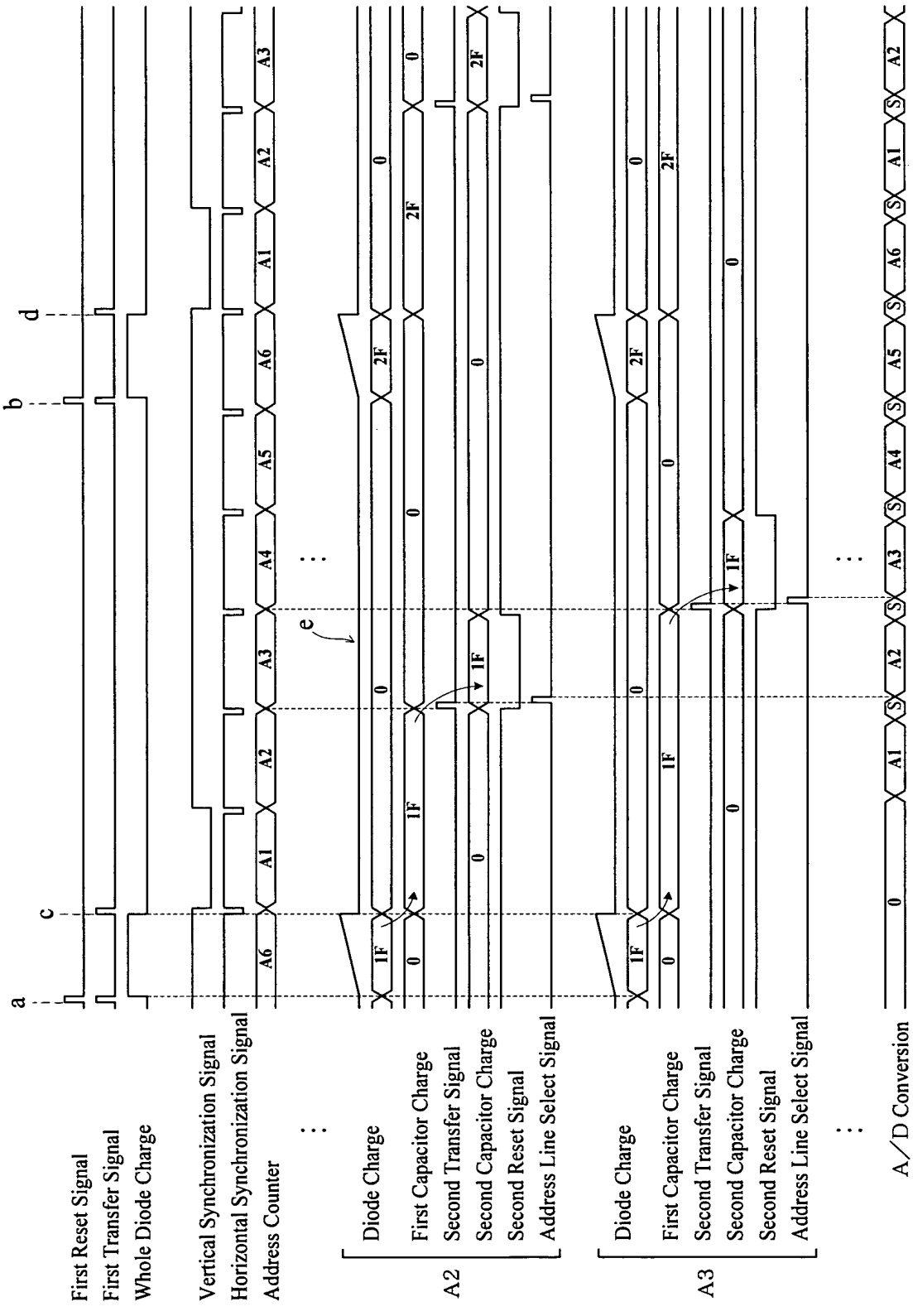

a
b
c
d
e
First Reset Signal
First Transfer Signal
Whole Diode Charge
Vertical Synchronization Signal
Horizontal Synchronization Signal
Address Counter
A2
Diode Charge
First Capacitor Charge
Second Transfer Signal
Second Capacitor Charge
Second Reset Signal
Address Line Select Signal
A3
Diode Charge
First Capacitor Charge
Second Transfer Signal
Second Capacitor Charge
Second Reset Signal
Address Line Select Signal
A/D Conversion
A6
A1
A2
A3
A4
A5
A6
A1
A2
A3
0
1F
2F
S

FIG.23

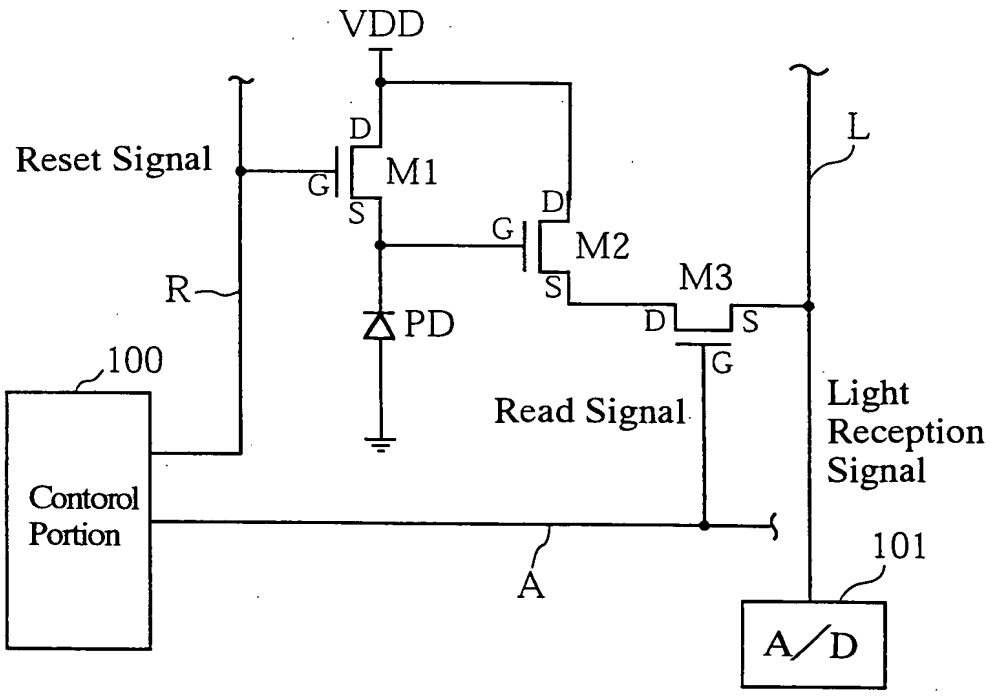

VDD
Reset Signal
D
G
M1
S
D
G
M2
S
M3
D
S
G
L
R
PD
100
Read Signal
Light
Reception
Signal
Contorol
Portion
A
101
A/D

FIG.24

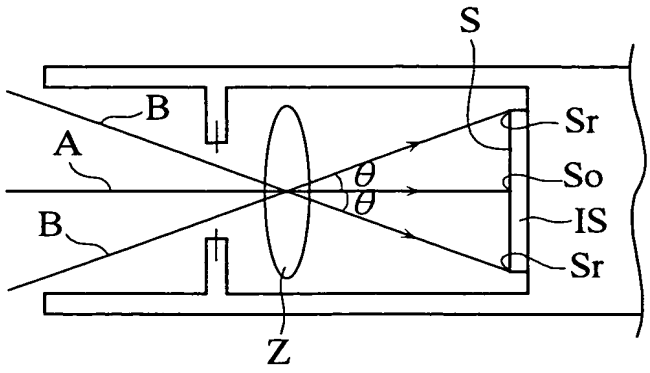

S
B
A
B
Sr
So
IS
Sr
θ
θ
Z

FIG.25

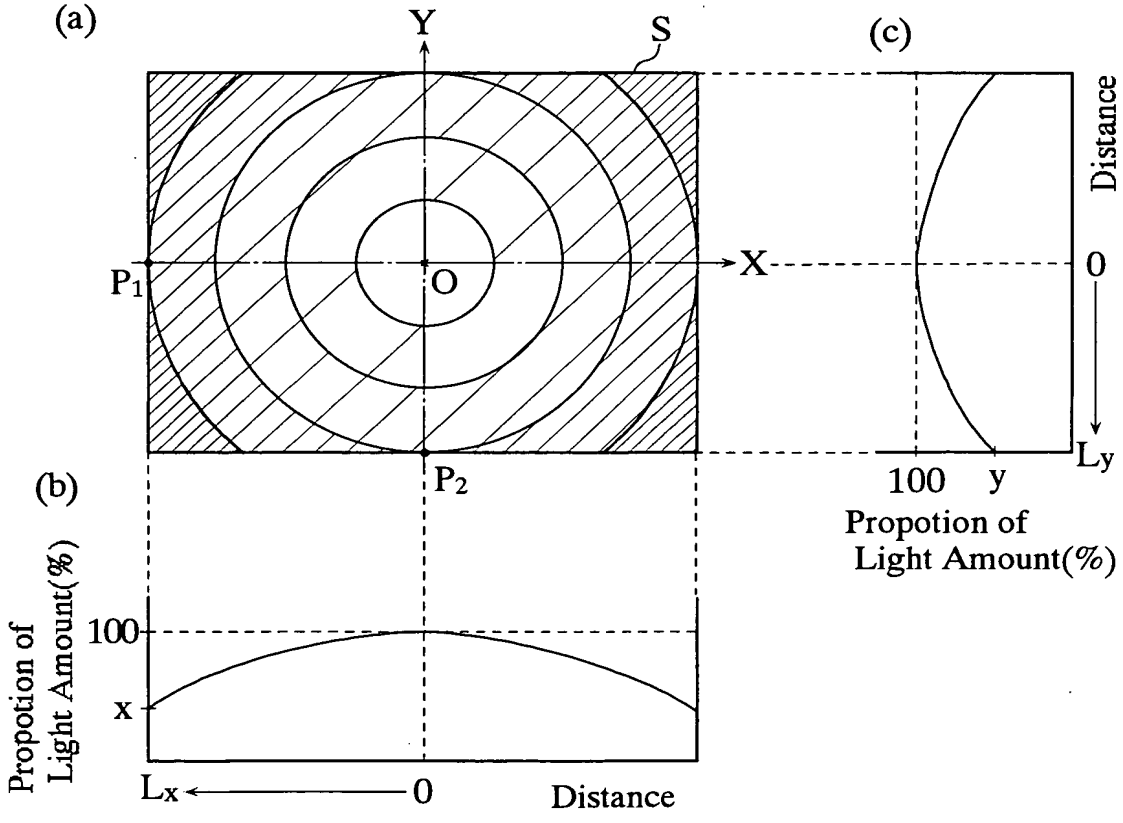
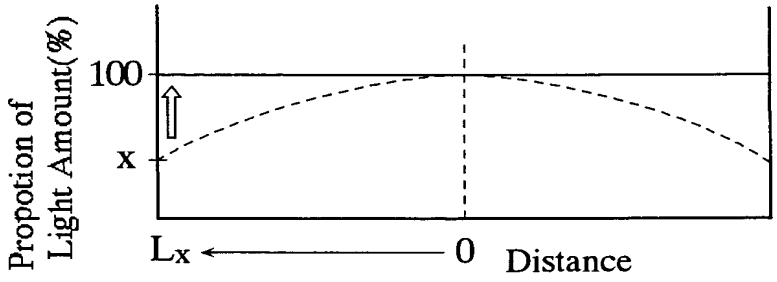

(a)
Y
S
X
O
P1
P2
(b)
Propotion of
Light Amount(%)
100
x
Lx
0
Distance
(c)
Distance
0
Ly
100
y
Propotion of
Light Amount(%)

FIG.26



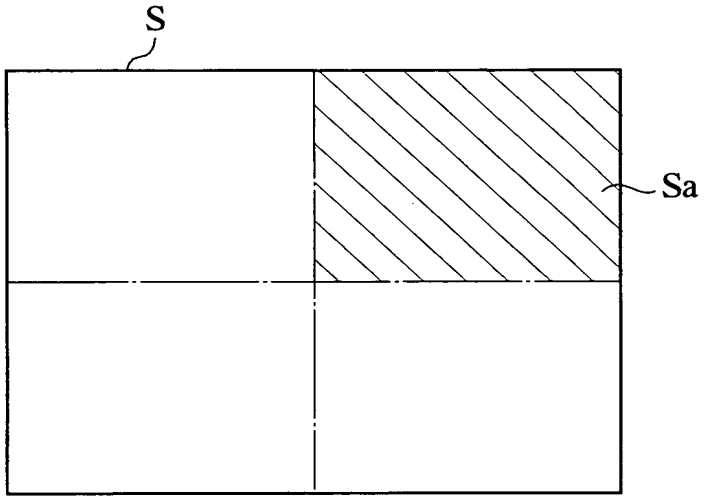


FIG.27